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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/780,330	02/17/2004	Gilbert Wolrich	10559-127002/P7866C	1102
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EXAMINER THAMMAVONG, PRASITH				
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary

Application No.

10/780,330

Applicant(s)

WOLRICH ET AL.

Examiner

PRASITH THAMMAVONG

Art Unit

2187

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 2/10/09, 5/28/08, and 10/18/07.
2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 28-45 is/are pending in the application.
4a) Of the above claim(s) _____ is/are withdrawn from consideration.
5) ☐ Claim(s) _____ is/are allowed.
6) ☒ Claim(s) 28-45 is/are rejected.
7) ☐ Claim(s) _____ is/are objected to.
8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-85/86)
Paper No(s)/Mail Date 5/28/08 and 10/18/07
4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date _____
5) ☐ Notice of Inventor's Patent Application
6) ☐ Other: _____

DETAILED ACTION

The Examiner acknowledges the applicant's submission of the amendment dated 2/10/09. At this point claims 28-29, 31, 34-36, 39-42, and 44-45 have been amended. Thus, claims 28-45 are pending in the instant application.

The instant application having Application No. 10/780,330 has a total of 18 claims pending in the application, there are 3 independent claims and 15 dependent claims, all of which are ready for examination by the examiner.

1. ACKNOWLEDGEMENT OF REFERENCES CITED BY APPLICANT

Information Disclosure Statement

As required by M.P.E.P. ' 609 (C), the applicant's submission of the Information Disclosure Statements, dated 10/18/07 and 5/28/08 , are acknowledged by the examiner and the cited references have been considered in the examination of the claims now pending. As required by M.P.E.P. ' 609 C(2), a copy of the PTOL-1449 initialed and dated by the examiner is attached to the instant office action.

2. REJECTIONS BASED ON PRIOR ART

Claim Rejections - 35 USC ' 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. ' 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a

patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claim 28-30, 32 and 34-43 are rejected under 35 U.S.C. 102(e) as being anticipated by Tremblay (US Patent # 6,212,604).

With respect to claim 28, the Tremblay reference teaches a processor, comprising:

multiple programmable units integrated within the processor; (fig. 3, element 306 and column 4, lines 7-29, where the registers are within the processors)

logic integrated within the processor to map resources within the multiple programmable units into a single address space, (column 4, lines 7-29, where the registers are mapped collectively to a address space in the instruction cache 212) the logic to provide data access to a resource within a first of the multiple programmable units to a second one of the multiple programmable units in response to a data access request of the second one of the multiple programmable units specifying an address within the single address space, (column 4, lines 7-29, where the instruction cache allows the processors to access data within the registers of the processors) wherein there is a one-to-one correspondence between respective addresses in the single address space and respective resources within the multiple programmable units. (column 4, lines 30-58, where there is one-to-one correlation between the registers specified in an instruction and the registers in P1 processor 208)

With respect to claim 29, the Tremblay reference teaches the processor of claim 28, wherein the resources within the multiple programmable units comprise register locations within the multiple programmable units. (column 4, lines 7-29, where the registers are programmed with address information)

With respect to claim 30, the Tremblay reference teaches the processor of claim 28, wherein the single address space comprises addresses corresponding to shared resources external to the multiple programmable units. (column 4, lines 7-29, where the registers store information about the instruction cache and/or main memory)

With respect to claim 32, the Tremblay reference teaches the processor of claim 28, wherein the multiple programmable units comprise multiple programmable multi-threaded units. (column 6, lines 14-45, where the registers can have multi-threaded instructions within them)

With respect to claim 34, the Tremblay reference teaches the processor of claim 28, wherein the logic comprises logic to receive a command from a programmable processor. (column 4, lines 7-29, where P2 processor 210 can issue commands as well)

With respect to claim 35, the Tremblay reference teaches the processor of claim 34, wherein the multiple programmable units comprise multiple programmable engines and the programmable processor. (column 4, lines 7-29, where P2 processor 208 can issue commands as well and where there is registers within the P2 processor 210)

With respect to claim 36, the Tremblay reference teaches a method, comprising:

mapping addresses in a single address space to resources within a set of multiple programmable units integrated within a processor, the single address space including addresses for different ones of the resources in different ones of the multiple programmable units; (column 4, lines 30-58, where there is one-to-one correlation between the registers specified in the instruction and the registers in P1 processor 208) and

providing data access to a resource within a first of the multiple programmable units to a second one of the multiple programmable units in response to a data access request of the second one of the multiple programmable units specifying an address within the single address space, (column 4, lines 7-29, where the instruction cache allows the processors to access data within the registers of the processors) wherein there is a one-to-one correspondence between respective addresses in the single address space and respective resources within the multiple programmable units. (column 4, lines 30-58, where there is one-to-one correlation between the registers specifies in an instruction and the registers in P1 processor 208)

With respect to claim 37, the Tremblay reference teaches the method of claim 36, further comprising receiving a command specifying the address in the single address space. (column 4, lines 7-29, where the registers are mapped collectively to a address space)

With respect to claim 38, the Tremblay reference teaches the method of claim 37, wherein the command comprises one selected from the following group: a read command and a write command. (column 7, lines 8-33, where the information is read from and stored into the registers)

With respect to claim 39, the Tremblay reference teaches the method of claim 37, wherein the receiving the command comprises receiving the command from a programmable processor. (column 4, lines 7-29, where P2 processor 210 can issue commands as well)

With respect to claim 40, the Tremblay reference teaches the method of claim 39, wherein the programmable processor comprises a programmable processor integrated within the processor; and wherein the multiple programmable units comprise multiple programmable engines and the programmable processor. (column 4, lines 7-29, where P2 processor 208 can issue commands as well and where there is registers within the P2 processor 210)

With respect to claim 41, the Tremblay reference teaches the method of claim 36, wherein the resources within the set of multiple programmable units comprises register locations within the multiple programmable units. (column 4, lines 7-29, where the registers are programmed with address information)

With respect to claim 42, the Tremblay reference teaches the method of claim 36, wherein the single address space comprises addresses corresponding to shared

resources external to the multiple programmable units. (column 4, lines 7-29, where the registers store information about the instruction cache and/or main memory)

With respect to claim 43, the Tremblay reference teaches the method of claim 36, wherein the multiple programmable units comprise multiple programmable multi-threaded units. (column 6, lines 14-45, where the registers can have multi-threaded instructions within them)

Claim Rejections - 35 USC ' 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claim 31 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tremblay (US Patent # 6,212,604) in view of Tran (US Patent # 6,138,240).

With respect to claim 31, the Tremblay reference teaches the processor of claim 30, wherein the shared resources external to the multiple programmable units comprise a memory internal to the processor and a randomly accessible memory external to the processor. (fig. 3, element 306 and 202; and column 4, lines 7-29, where the registers store information about the instruction cache and/or main memory)

However, the Tremblay reference does not explicitly teach and a Peripheral Component Interconnect (PCI) unit.

The Tran reference does teach that is conventional to have a Peripheral Component Interconnect (PCI) unit. (column 4, lines 37-49)

The Tremblay and Short references are analogous art because they are in the same field of endeavor of memory access and control.

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to modify the Tremblay reference to have a Peripheral Component Interconnect (PCI) unit, which is taught by the Tran reference.

The suggestion/motivation for doing so would have been to allow high speed access for peripherals. (Tran, column 4, lines 37-49)

Therefore it would have been obvious to combine the teachings of Tremblay reference with the tran reference for the benefit of high speed access to obtain the invention as specified in claim 31.

Claims 33 and 44 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tremblay (US Patent # 6,212,604) in view of Short (US Patent # 5,633,865).

With respect to claim 33, the Tremblay reference does not explicitly teach there is an interface to a media access controller (MAC).

The Short reference does teach that is conventional to have an interface to a media access controller (MAC). (column 3, lines 4-31)

The Tremblay and Short references are analogous art because they are in the

same field of endeavor of memory access and control.

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to modify the Tremblay reference to have an interface to a media access controller (MAC), which is taught by the Short reference.

The suggestion/motivation for doing so would have been to allow access to networks via the MAC (column 3, lines 4-31).

Therefore it would have been obvious to combine the teachings of Tremblay reference with the Short reference for the benefit of network access to obtain the invention as specified in claim 33.

With respect to claim 44, the Tremblay reference teaches a device, comprising:
at least one processor, (see fig. 3, elements 208 and 210) the processor
comprising:

multiple programmable units; (column 6, lines 14-45, where the registers can have multi-threaded instructions within them) and

logic to map resources within the multiple programmable units and resources external to the multiple programmable units into a single address space, the resources within the multiple programmable units comprising register locations, (column 4, lines 7-29, where the registers are mapped collectively to a address space) the resources external to the multiple programmable units comprising at least one Random Access Memory (RAM) external to the processor, (column 4, lines 7-29, where the registers store information about the instruction cache and/or main memory) the logic to provide data access to a resource within a first of the

multiple programmable units to a second one of the multiple programmable units in response to a data access request of the second one of the multiple programmable units specifying an address within the single address space, (column 4, lines 7-29, where the instruction cache allows the processors to access data within the registers of the processors) wherein there is a one-to-one correspondence between respective addresses in the single address space and respective resources within the multiple programmable units. (column 4, lines 30-58, where there is one-to-one correlation between the registers specifies in an instruction and the registers in P1 processor 208)

However, the Tremblay reference does not explicitly teach that there is at least one media access controller (MAC) coupled to the at least one processor.

The Short reference does teach that it is conventional to have there be at least one media access controller (MAC) coupled to the at least one processor. (column 3, lines 4-31)

The Tremblay and Short references are analogous art because they are in the same field of endeavor of memory access and control.

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to modify the Tremblay reference to have at least one media access controller (MAC) coupled to the at least one processor, which is taught by the Short reference.

The suggestion/motivation for doing so would have been to allow access to networks via the MAC (column 3, lines 4-31).

Therefore it would have been obvious to combine the teachings of Tremblay reference with the Short reference for the benefit of network access to obtain the invention as specified in claim 44.

Claim 45 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tremblay (US Patent # 6,212,604) in view of Short (US Patent # 5,633,865) as applied to claim 44 above, and further in view of Orton et al.(US Patent # 5,379,432).

With respect to claim 45, the Tremblay reference teaches the processor further comprises a programmable processor integrated within the processor. (column 4, lines 7-29, where P2 processor 210 can issue commands as well)

However, the combination of the Tremblay and Short references does not explicitly teach that the programmable processor has a different architecture than the multiple programmable units.

The Orton reference does teach that the programmable processor has a different architecture than the multiple programmable units. (column 13, line 51 to column 14, line 2)

The Tremblay, Short, and Orton references are analogous art because they are in the same field of endeavor of memory access and control.

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to modify the combination of the Tremblay and Short references to have the programmable processor to be a different architecture than the multiple programmable units, which is taught by the Orton reference.

The suggestion/motivation for doing so would have been to allow access for processors of different architectures to share the same address space. (column 13, line 51 to column 14, line 2)

Therefore it would have been obvious to combine the teachings of Tremblay, Short, and Orton references for the benefit of shared memory to obtain the invention as specified in claim 45.

5. ARGUMENTS CONCERNING NON-PRIOR ART REJECTIONS/OBJECTIONS

Rejections - USC 112

Applicant's arguments/amendments with respect to claims 35 and 44-45 have been considered and have overcome the Examiner's prior rejections and thus are withdrawn.

6. ARGUMENTS CONCERNING PRIOR ART REJECTIONS

Rejections - USC 102/103

Applicant's arguments pertaining to claim 28 and its dependent claims:

Applicant argues:

The Office Action rejected claim 28 based on Tremblay (U.S. Pat. No. 6,212,604). Tremblay describes two processors, P1 and P2. However, Tremblay does not describe that either processor can access the other processor's internal resources by specifying an address in a single address space. That is, for example, Tremblay does not describe that P1 can access the internal registers of P2 via a data request specifying an address in an address space that spans the internal registers of P1 and P2, or vice versa. As such, Applicant respectfully requests withdrawal of the rejection of claim 28, and for at least the same reason, its corresponding dependent claims.

Examiner's Response:

Applicant's arguments have been considered but are not persuasive. The Examiner contends that the Tremblay reference teaches that limitations of "the logic to provide data access to a resource within a first of the multiple programmable units to a second one of the multiple programmable units in response to a data access request of the second one of the multiple programmable units specifying an address within the single address space, wherein there is a one-to-one correspondence between respective addresses in the single address space and respective resources within the multiple programmable units". Column 4, lines 7-29 of the Tremblay reference clearly teaches the use of the instruction cache to allow the processors to access data within the registers of the processors when accessing a cached instruction, thus anticipating the applicant's limitation "the logic to provide data access to a resource within a first of the multiple programmable units to a second one of the multiple programmable units in response to a data access request of the second one of the multiple programmable units specifying an address within the single address space". Column 4, lines 30-58 of the Tremblay reference also teaches a one-to-one correlation between the registers specified in an instruction and the registers in P1 processor 208, thus anticipating the applicant's limitation of "wherein there is a one-to-one correspondence between respective addresses in the single address space and respective resources within the multiple programmable units". Thus, the Examiner contends that the Tremblay reference teaches the limitations above as instantly and broadly claimed.

Applicant's arguments pertaining to claim 36 and 45 and its dependent claims:

Applicant argues:

Independent claims 36 and 45 have been amended to include recitation of a similar limitation. Thus, for at least the same reason, Applicant also respectfully requests withdrawal of the rejection of independent claims 36 and 45 and their corresponding dependent claims.

Examiner's Response:

See response above.

8. CLOSING COMMENTS

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

a. STATUS OF CLAIMS IN THE APPLICATION

The following is a summary of the treatment and status of all claims in the application as recommended by **M.P.E.P. ' 707.07(i)**:

a(1) CLAIMS REJECTED IN THE APPLICATION

Per the instant office action, claims 28-45 have received a second action on the merits and are subject of a second action final.

b. DIRECTION OF FUTURE CORRESPONDENCES

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Prasith Thammavong whose telephone number is (571) 270-1040 can normally be reached on Monday - Thursday 9:00am - 6:00pm and the first Friday of the bi-week, 9:00 am –5:00 pm

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kevin Ellis can be reached on (571) 272-4205. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Prasith Thammavong/
Patent Examiner
Art Unit 2187
May 13, 2009

/Kevin L Ellis/
Acting SPE of Art Unit 2187